

Copy

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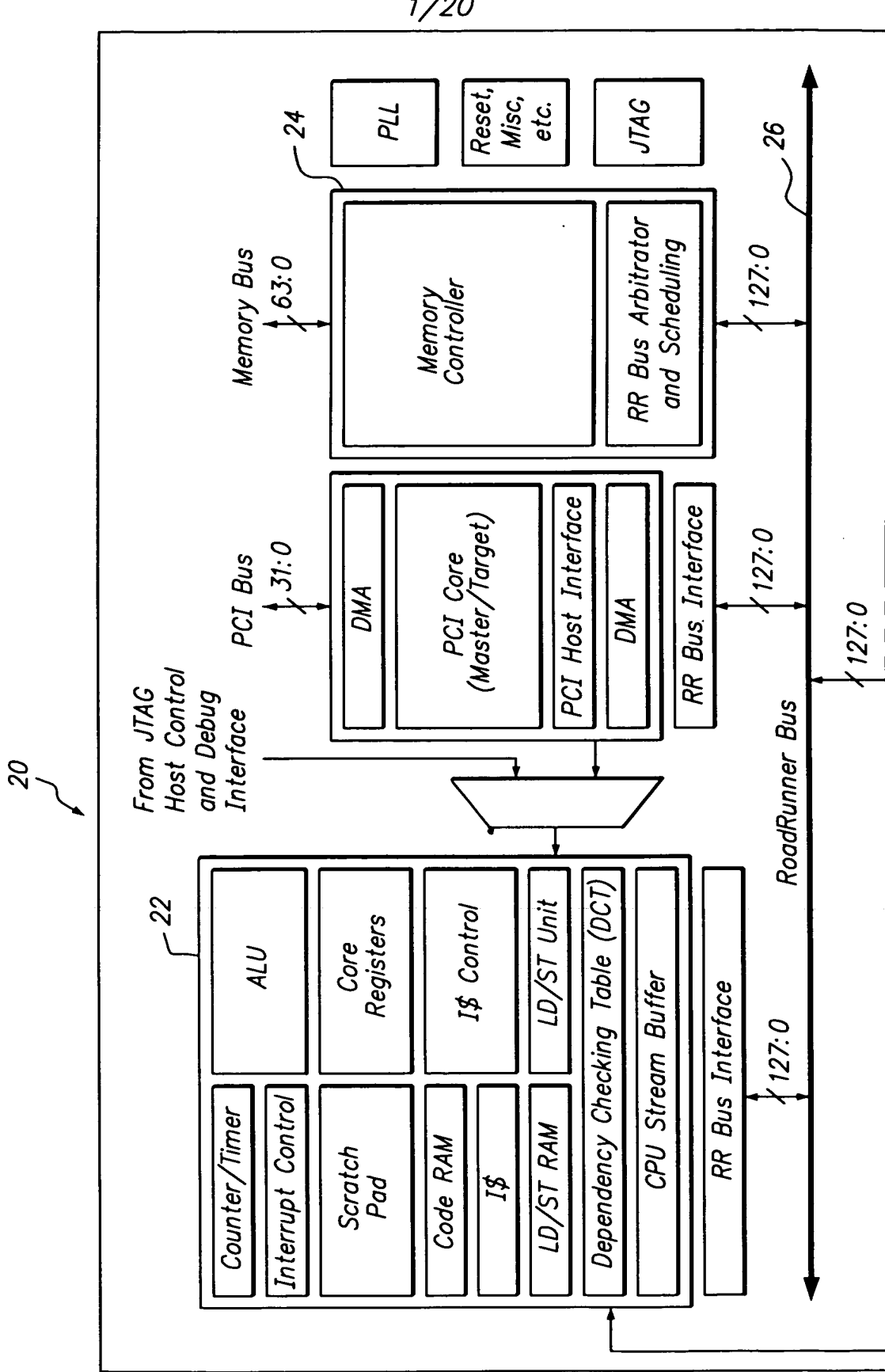


FIG. 1A

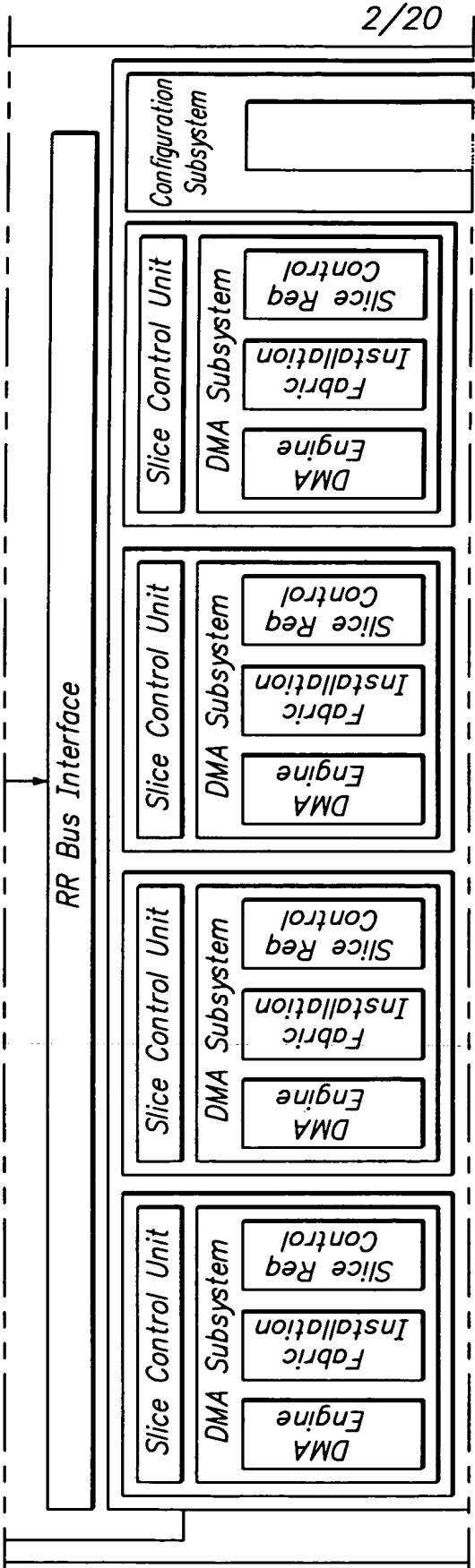
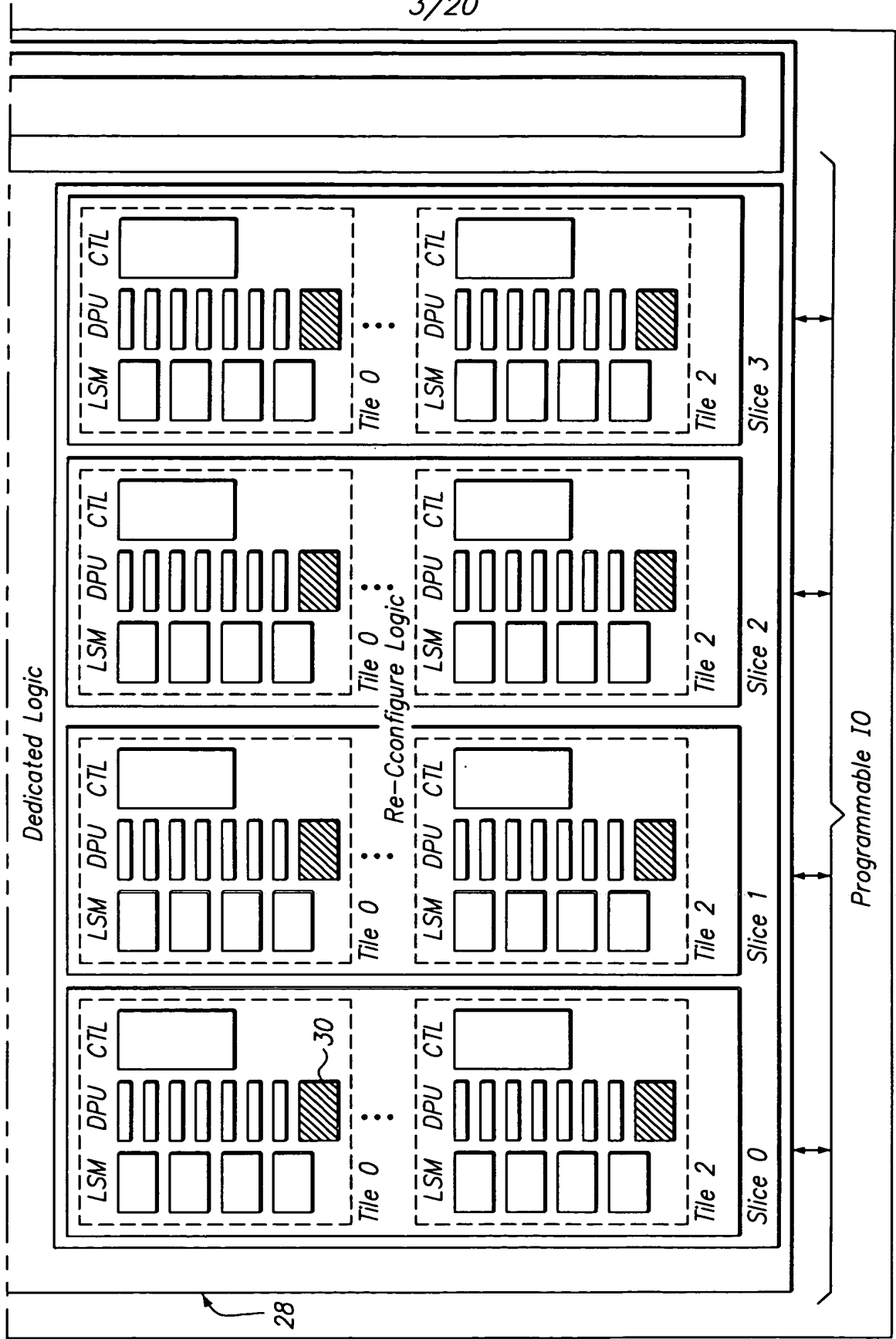


FIG. 1B

FIG. 1

FIG. 1A	FIG. 1B	FIG. 1C
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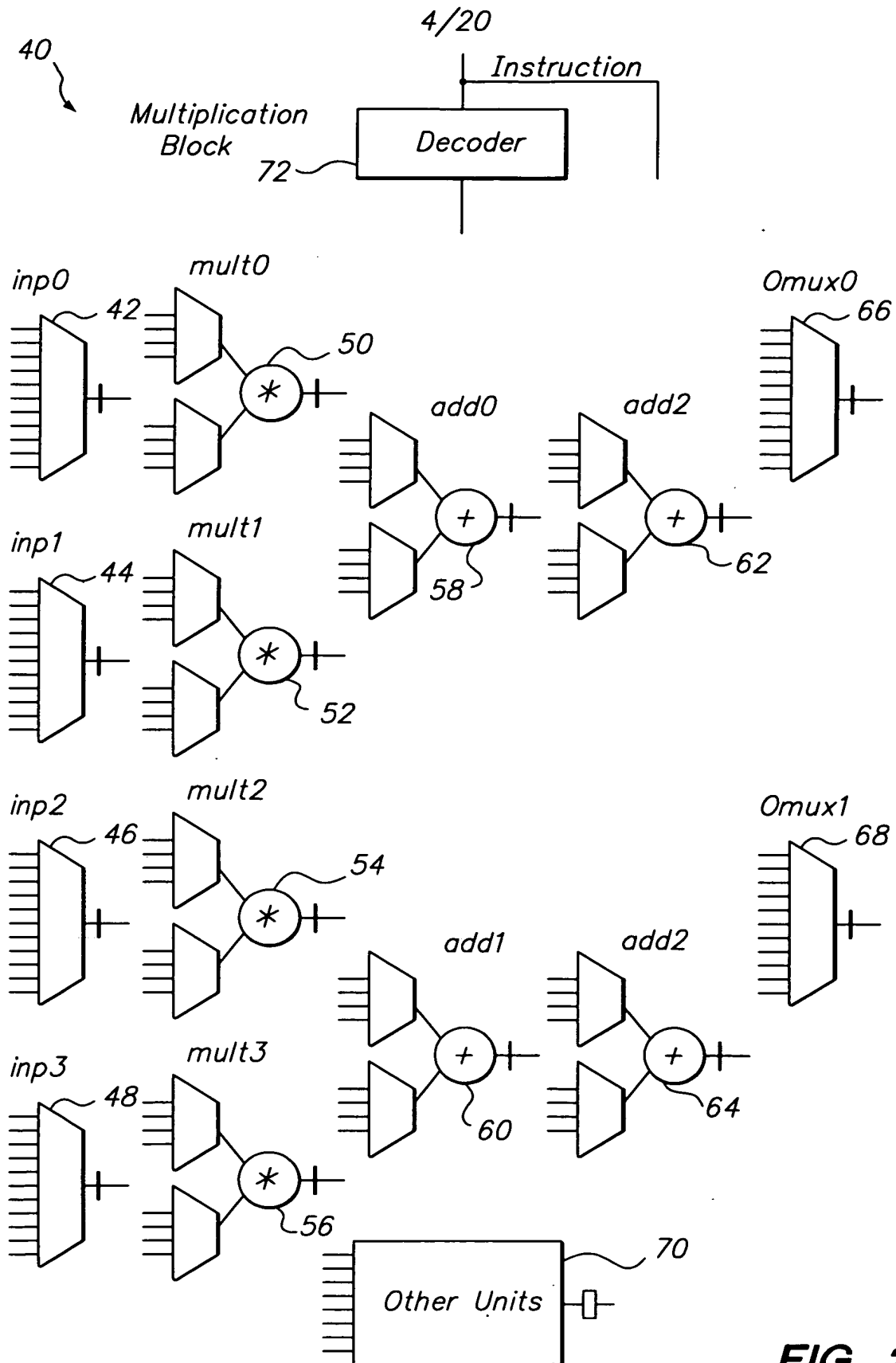


FIG. 2

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2MULT-CS2112 Compatible mode 2 independent multipliers

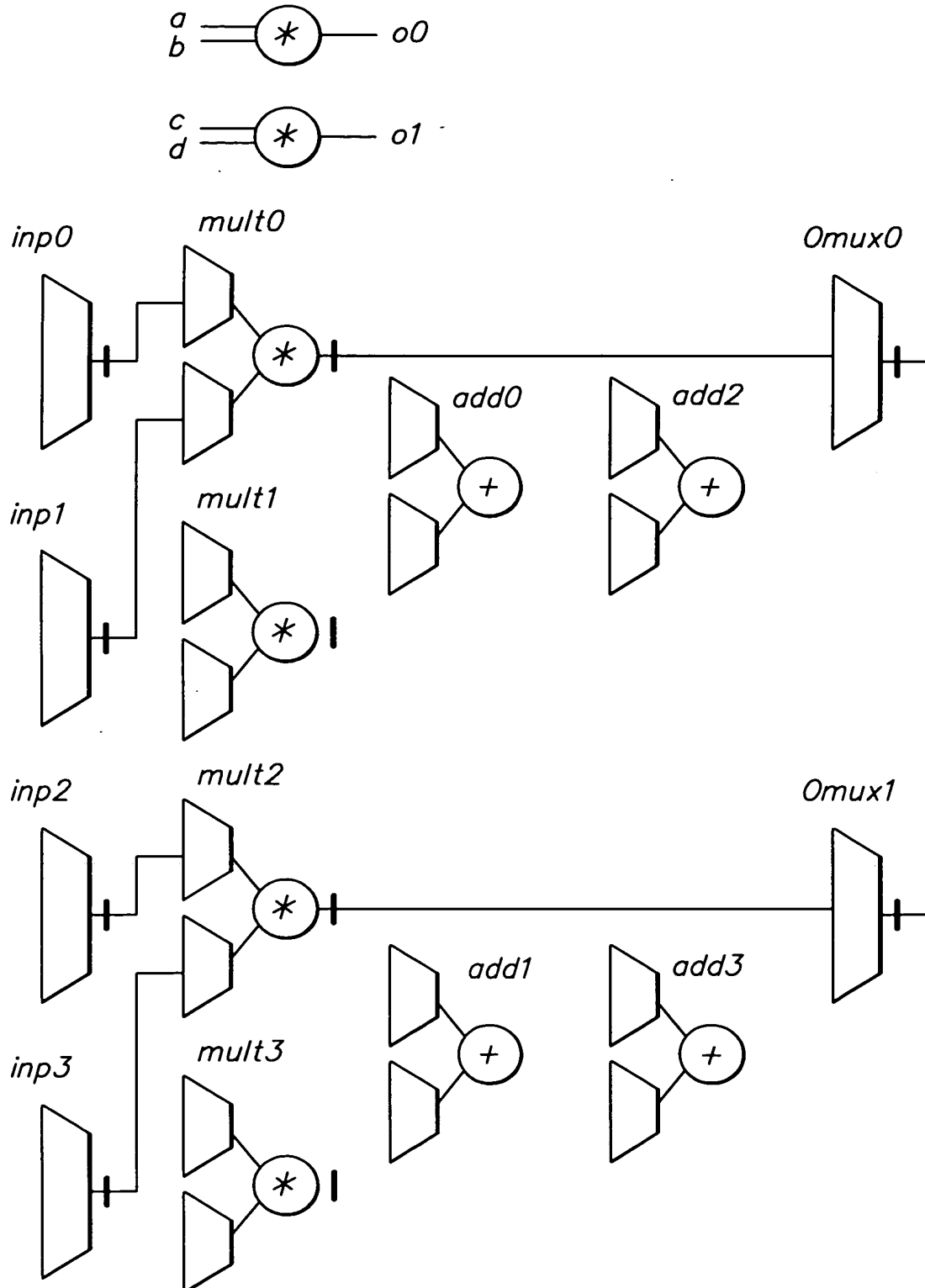


FIG. 3A

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4ADD32—Sum of 4 32-bit inputs

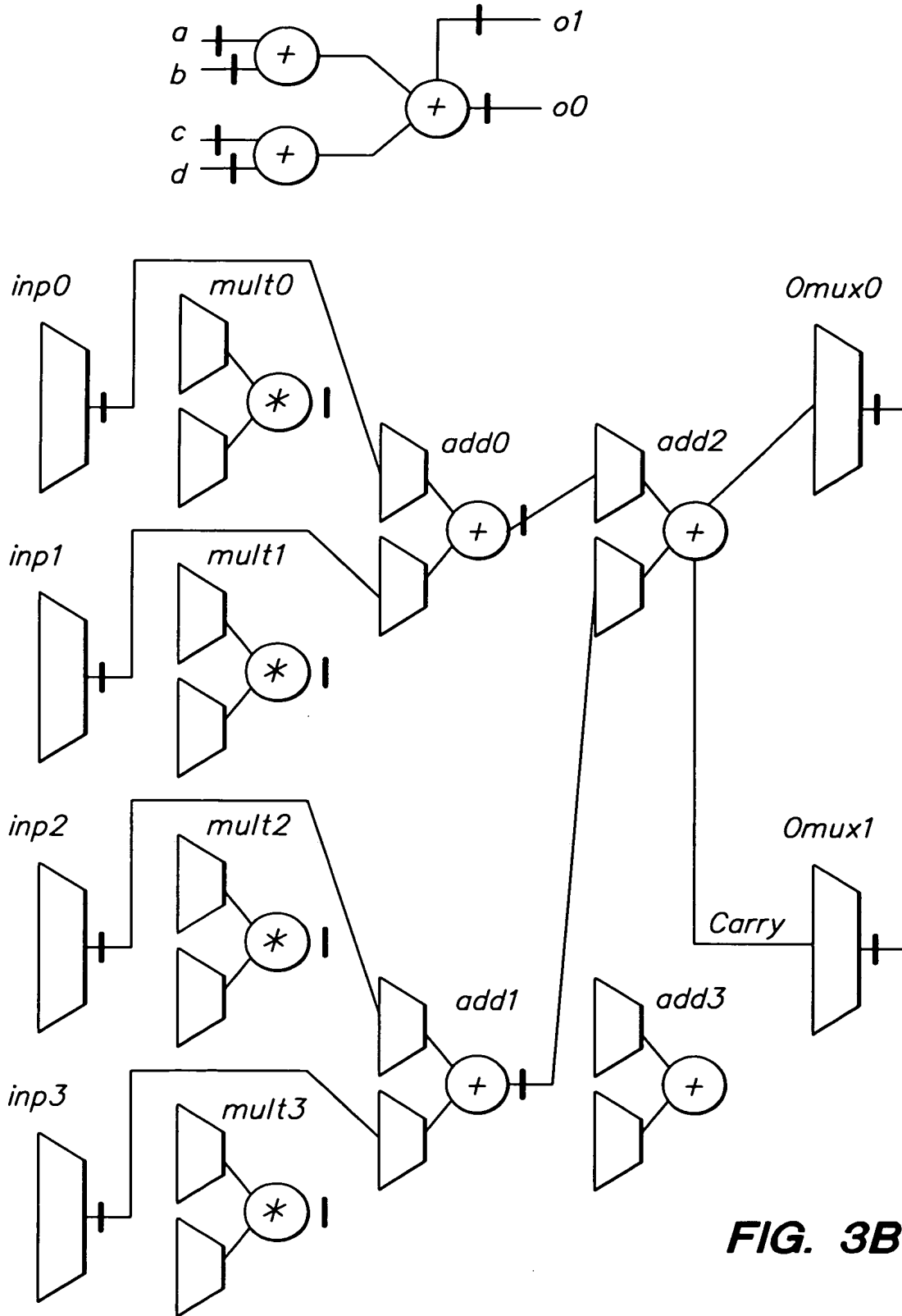


FIG. 3B

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4ADD16—Sum of 4 packed 16-bit inputs, sum of upper, lower 16-bits

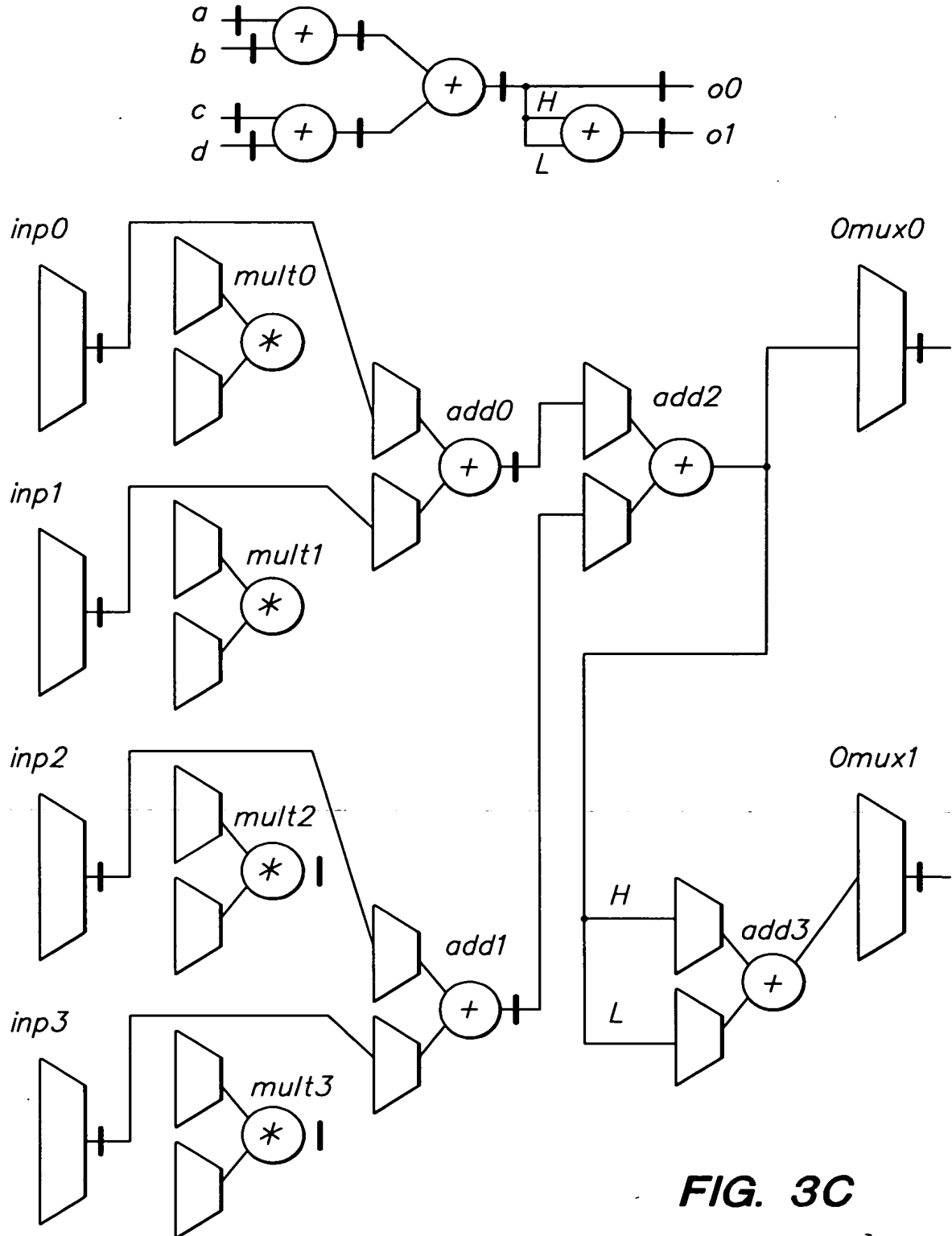


FIG. 3C

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4MULT-4 multipliers with pack 16-bit inputs

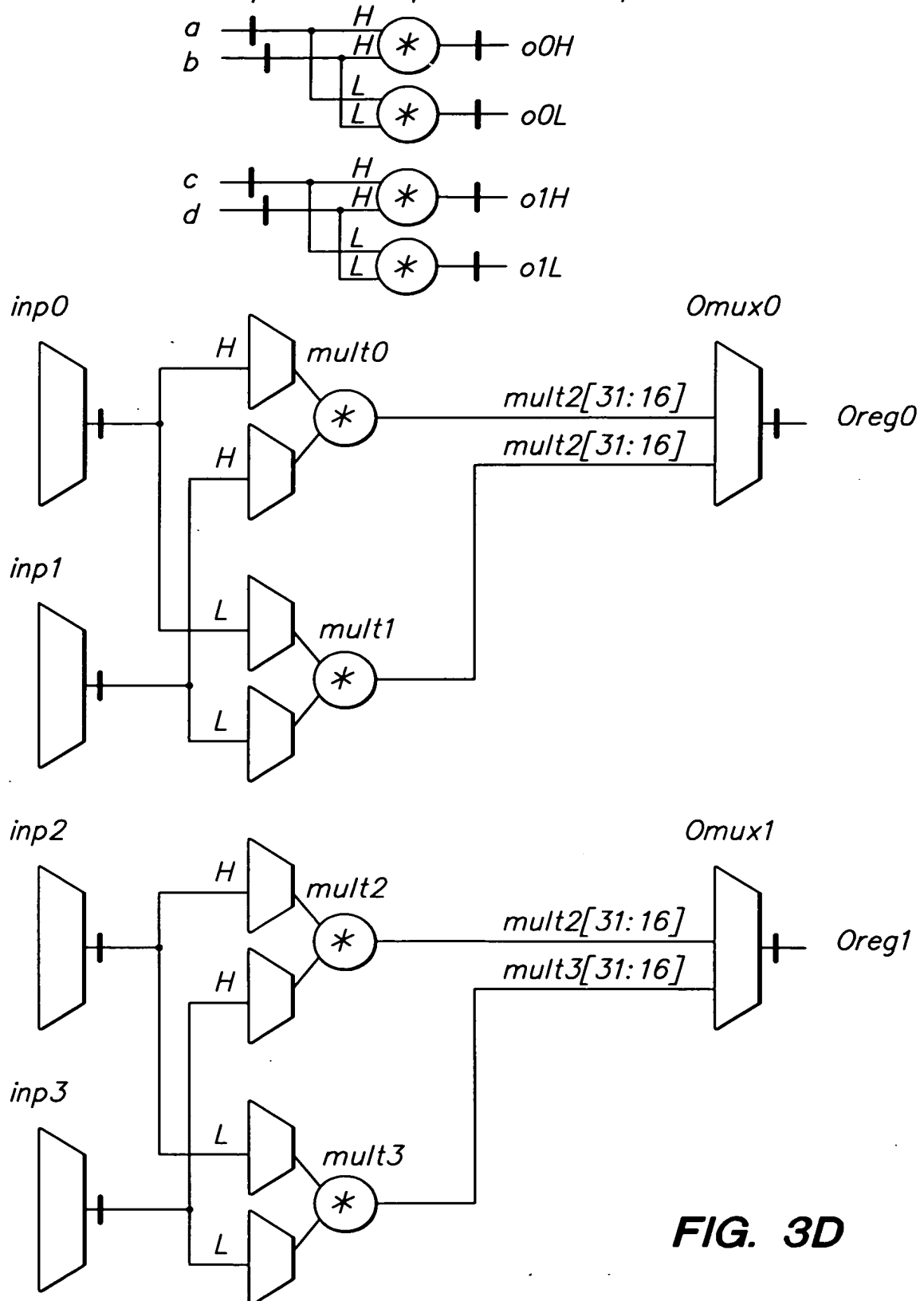


FIG. 3D

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4MULTSUM—Sum of 4 multipliers

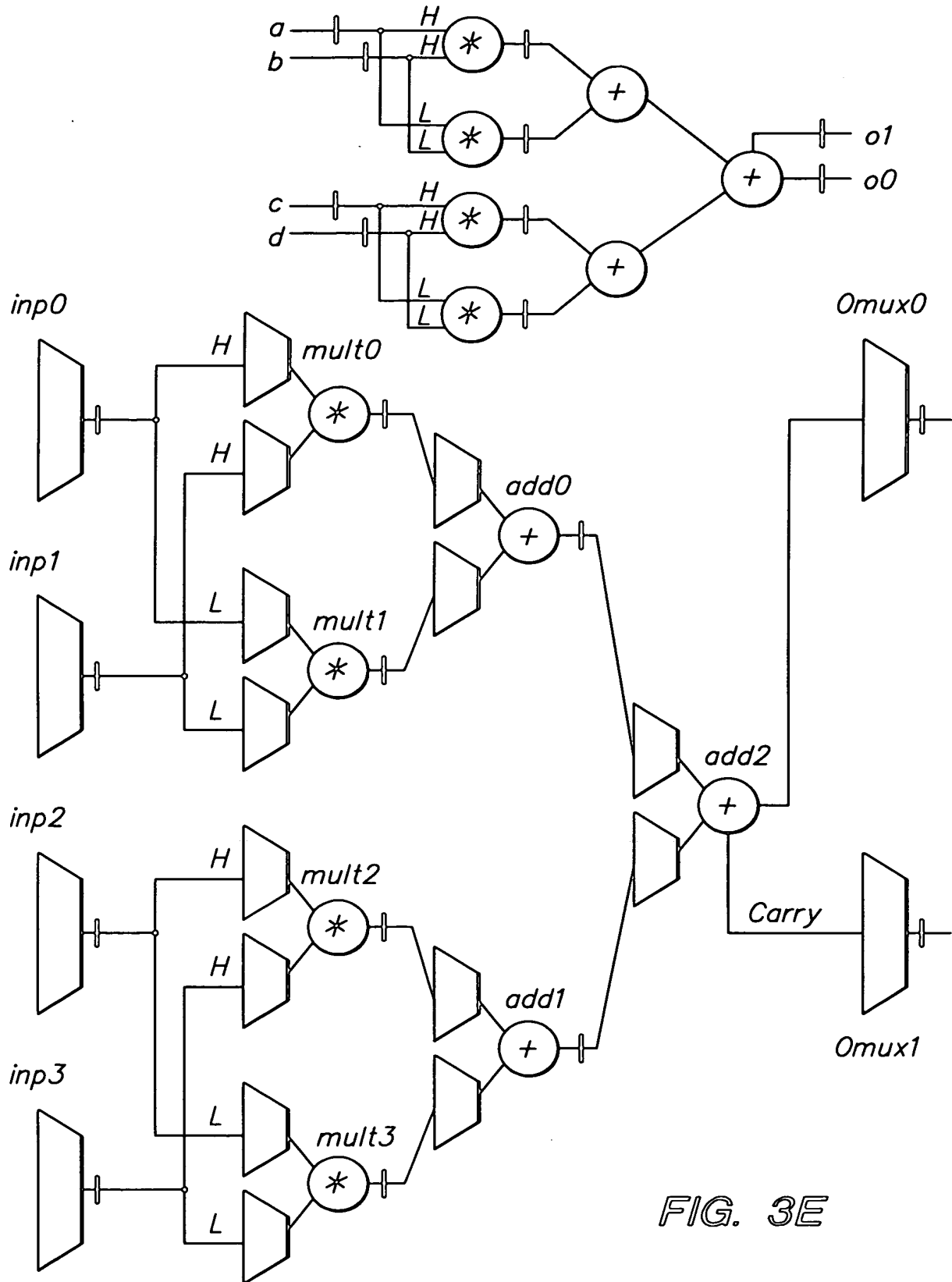


FIG. 3E

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4MULT2SUM-2 Sums of 2 multipliers

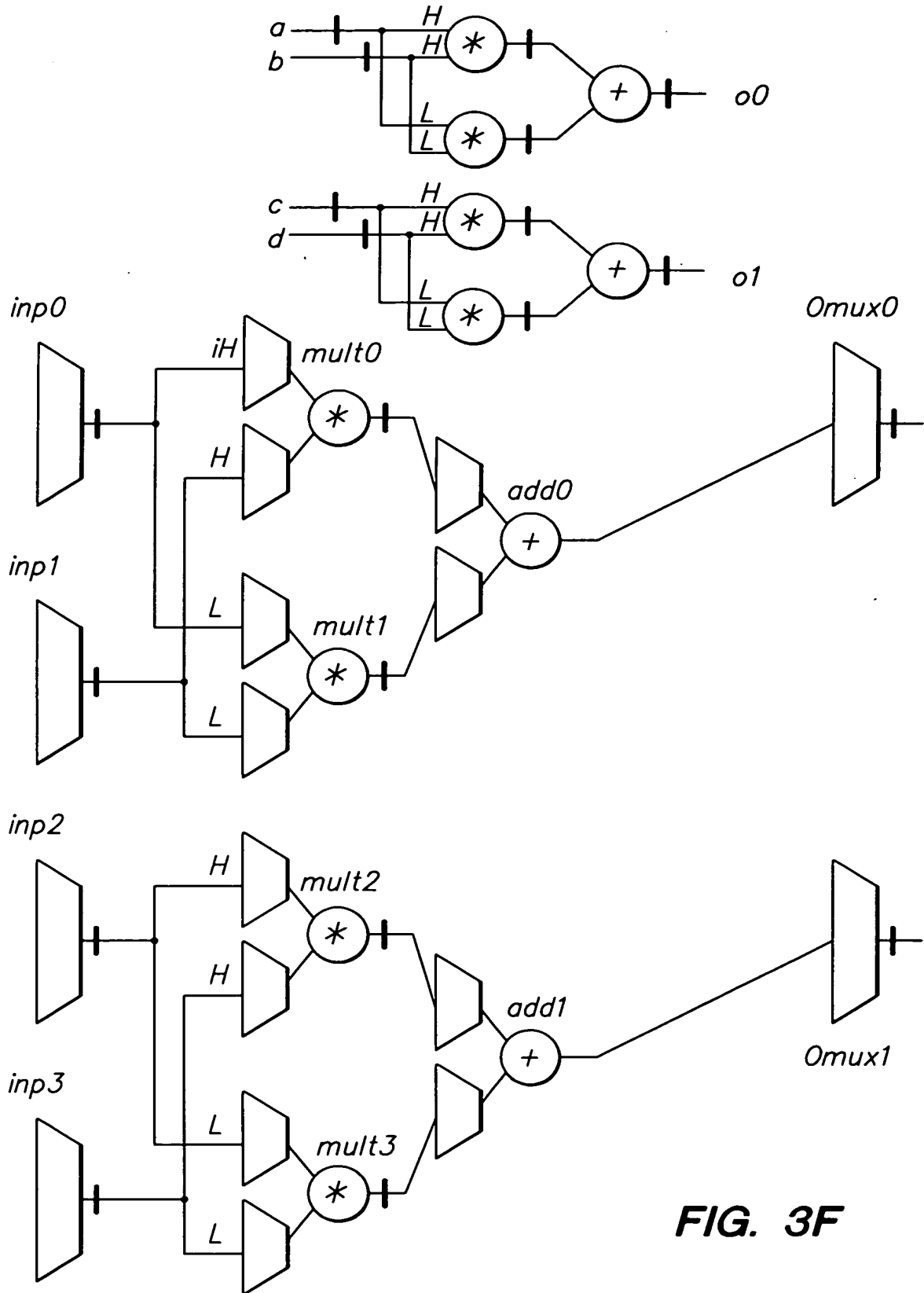


FIG. 3F

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CMULT-32-bit output complex multiply with 32-Bit accumulation
 input, Assumes real part in High 16-bits, imaginary in Low 16-bits

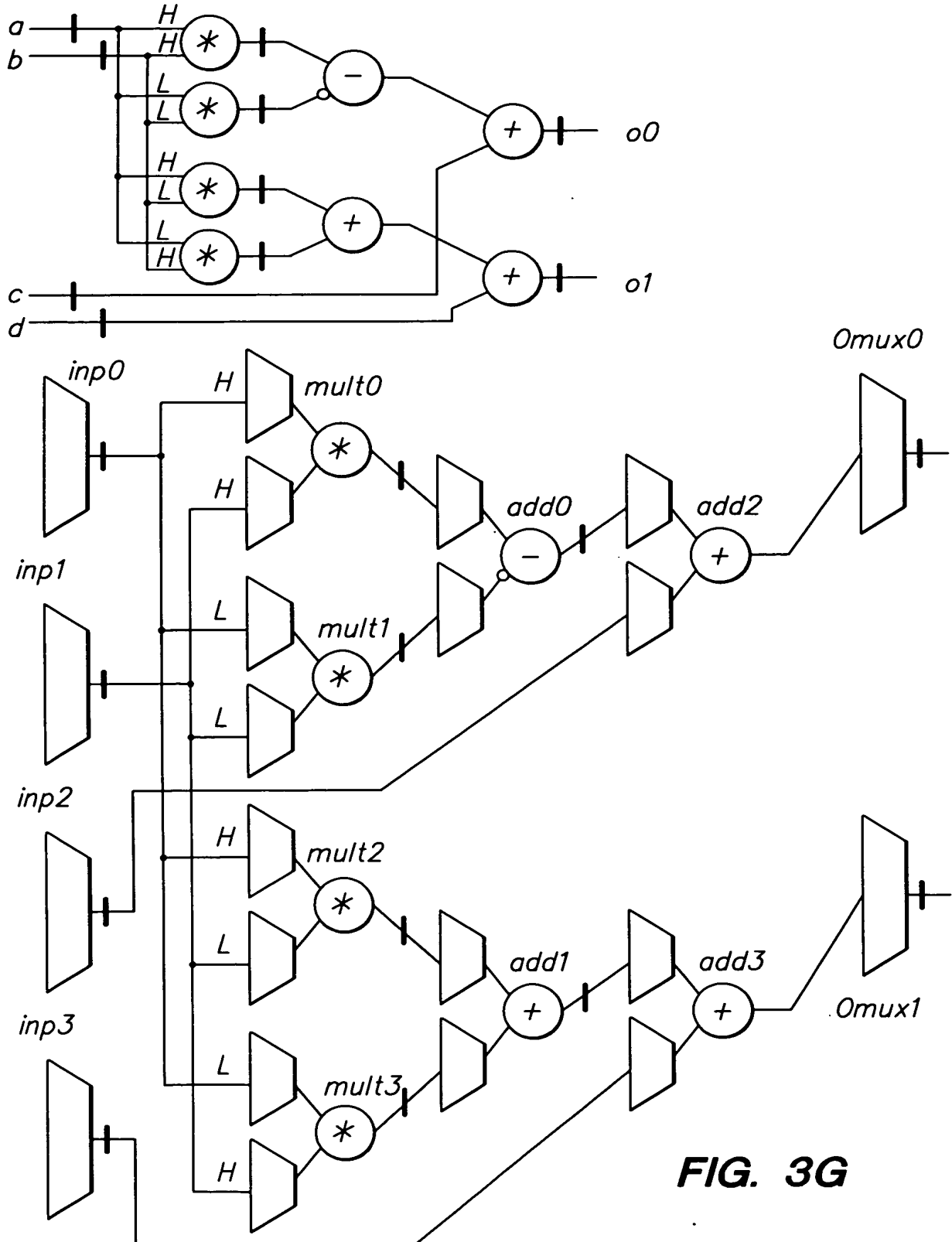


FIG. 3G

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CMULT16—Complex Multiplier with 16-Bit Packed data, and indepent
 delay path. Assumes real part in High 16-bits, imaginary in Low
 16-bits

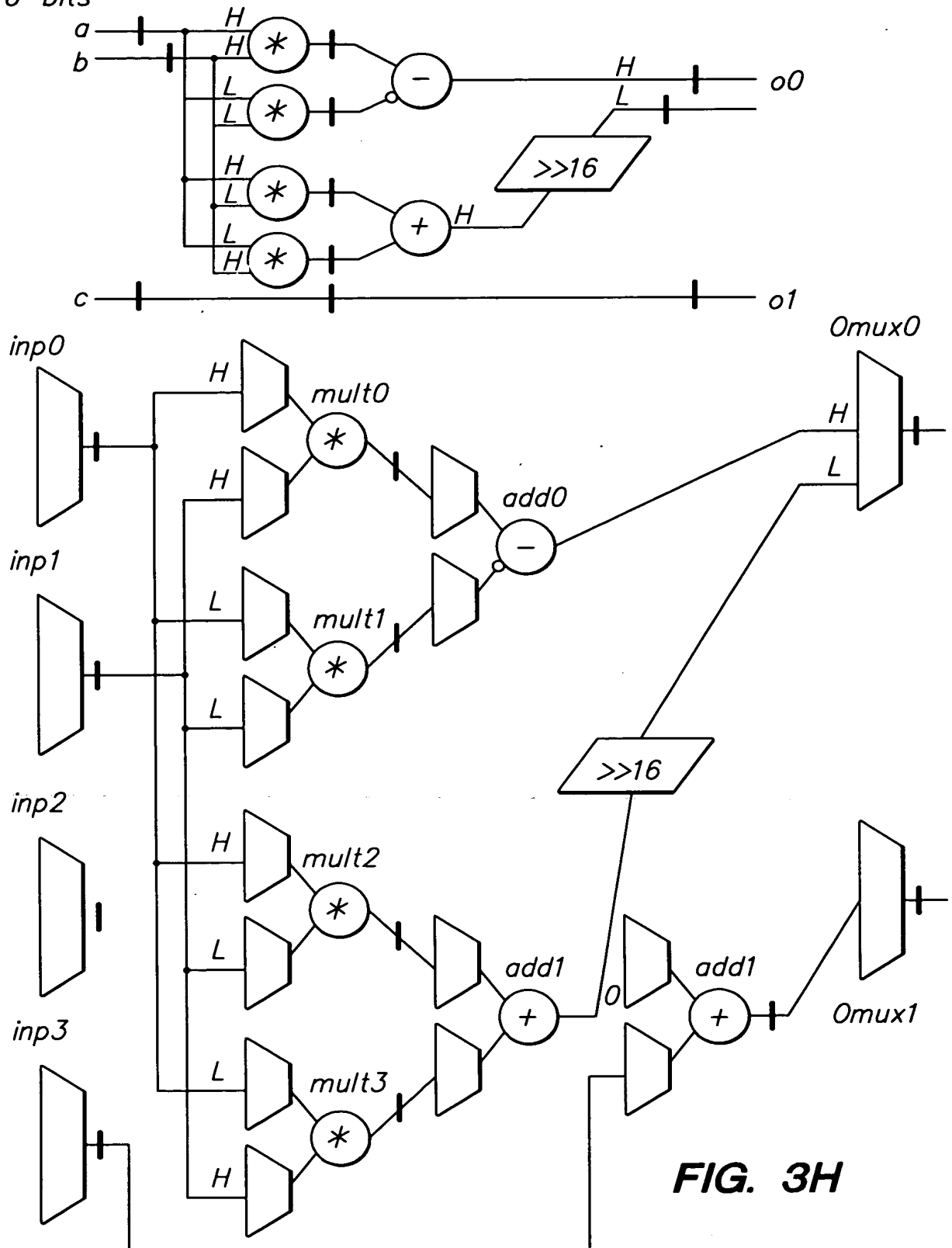


FIG. 3H

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4FIR-4 tap FIR filter

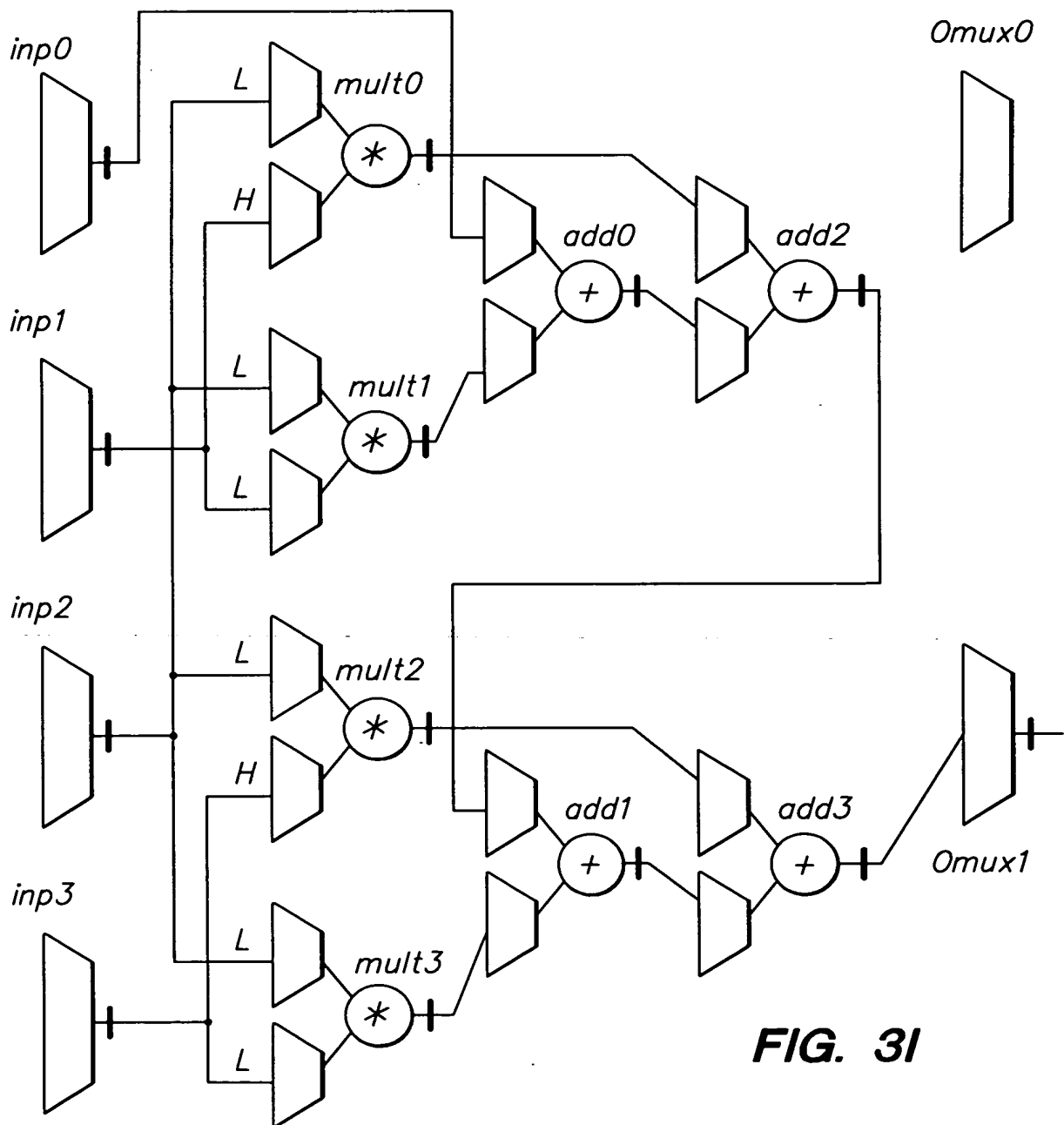
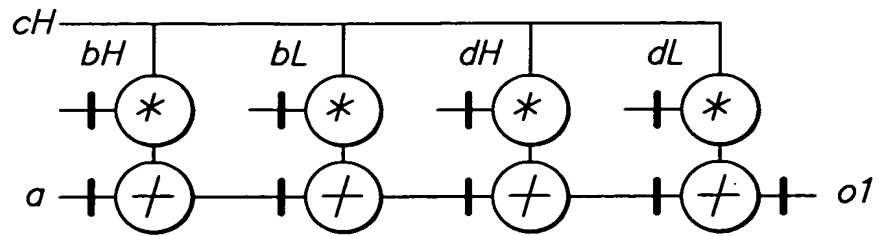
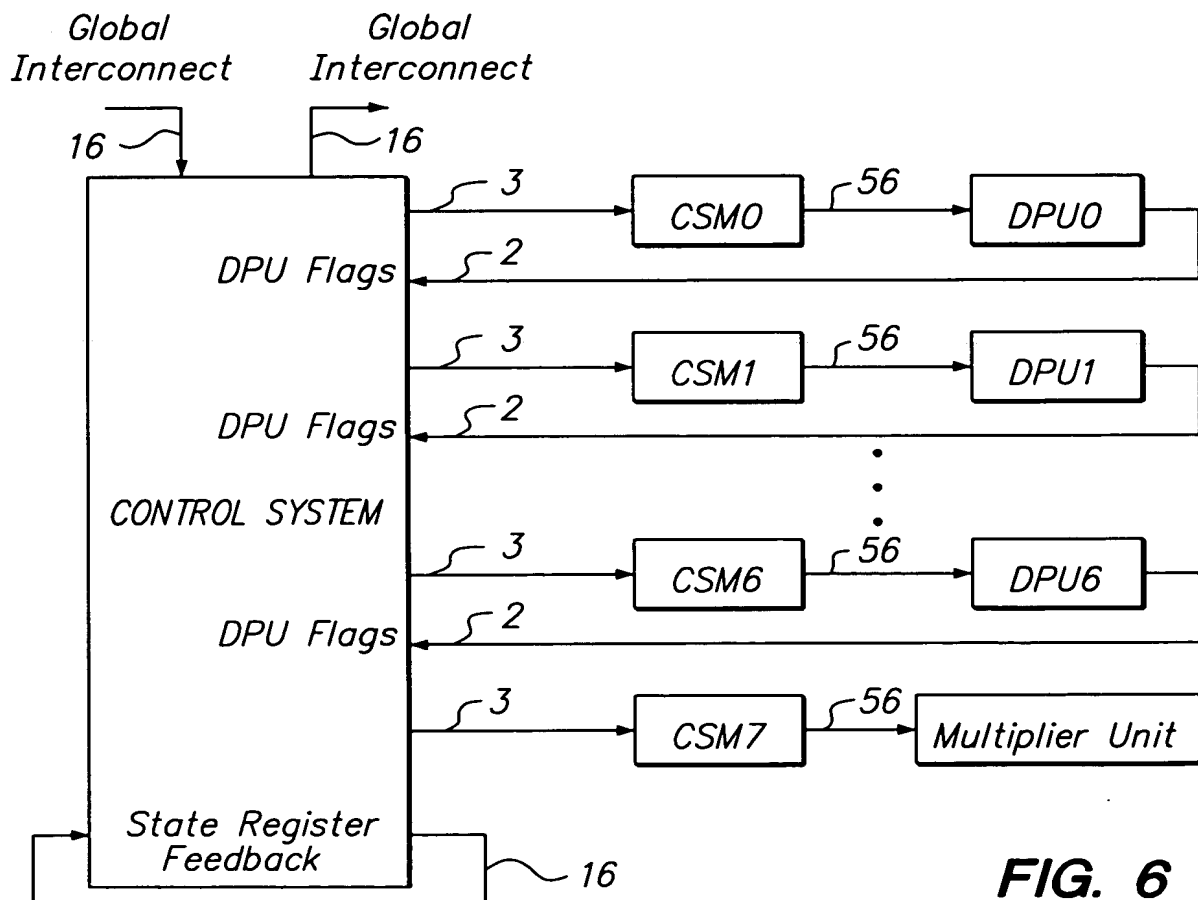
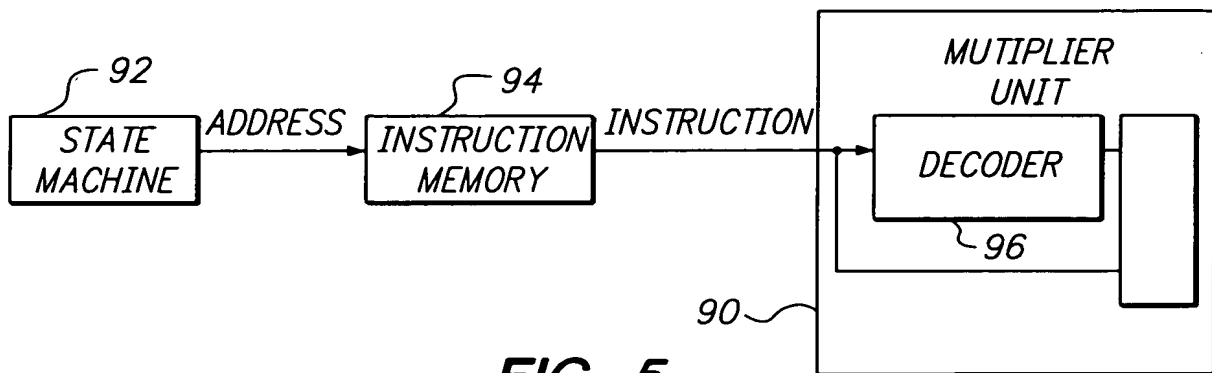
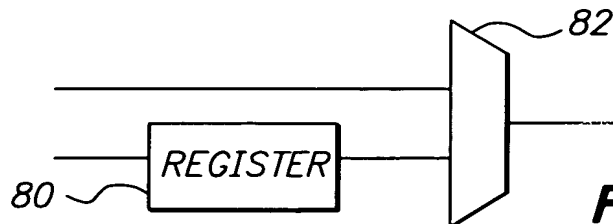


FIG. 31

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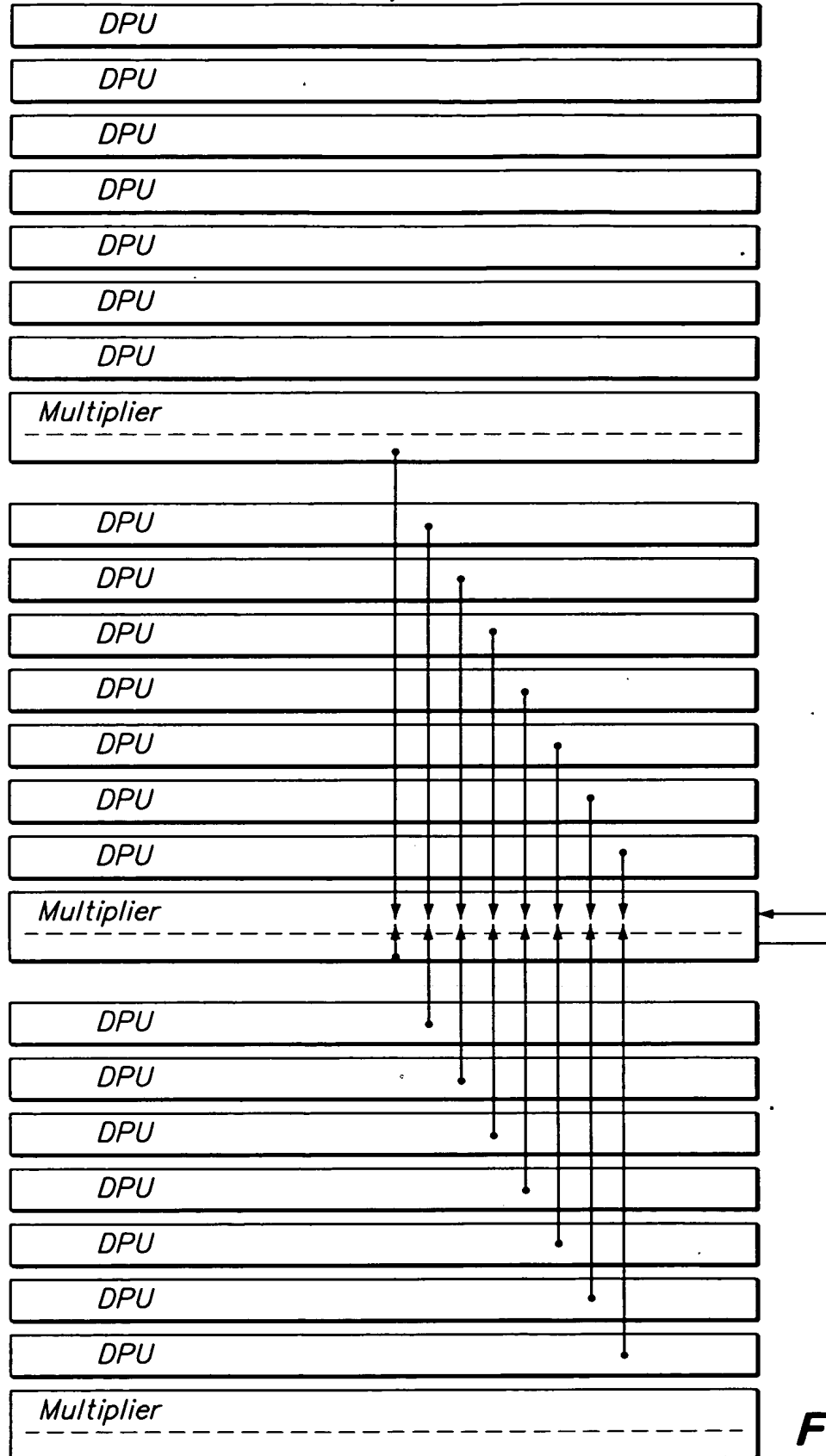


FIG. 7

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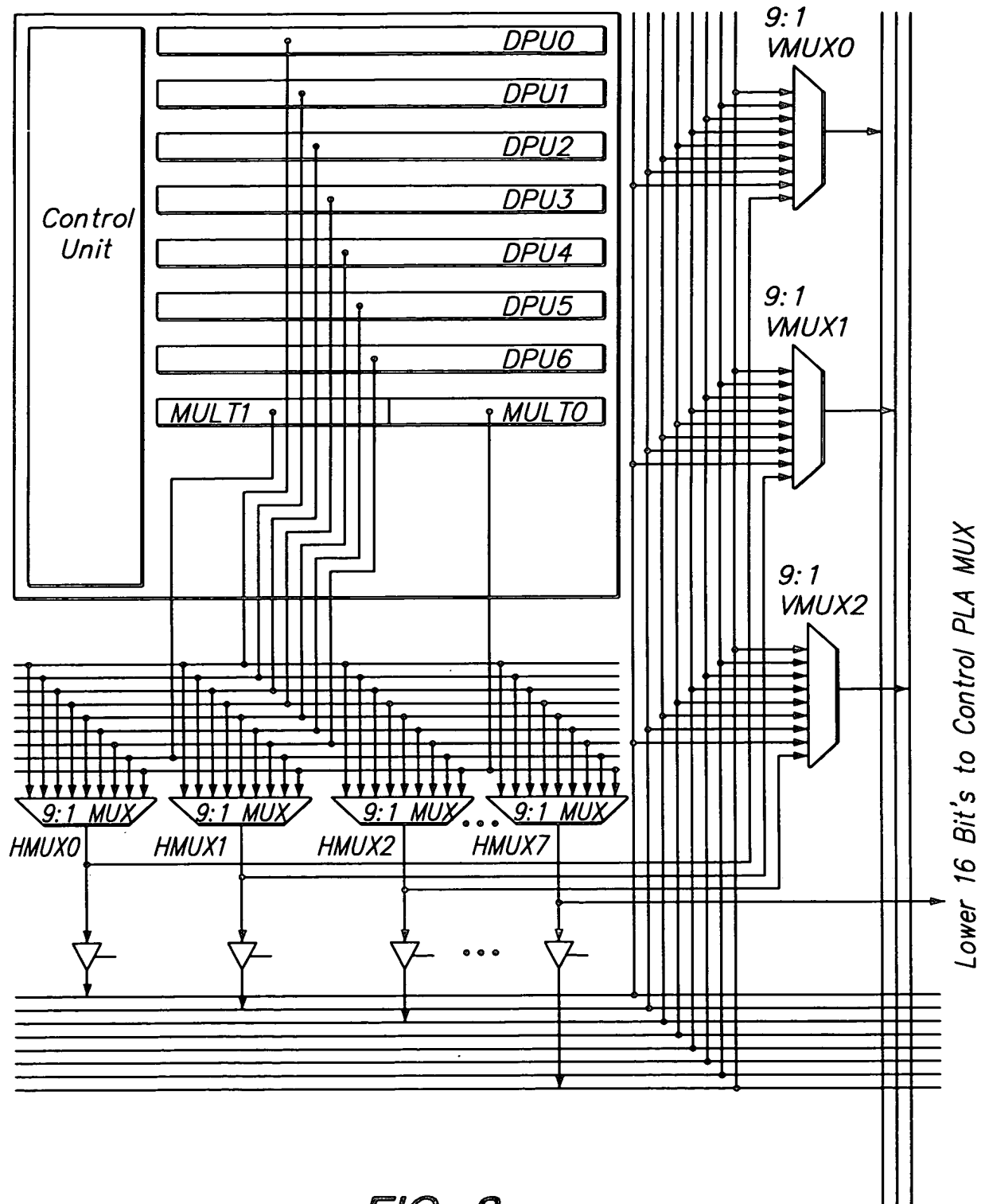


FIG. 8

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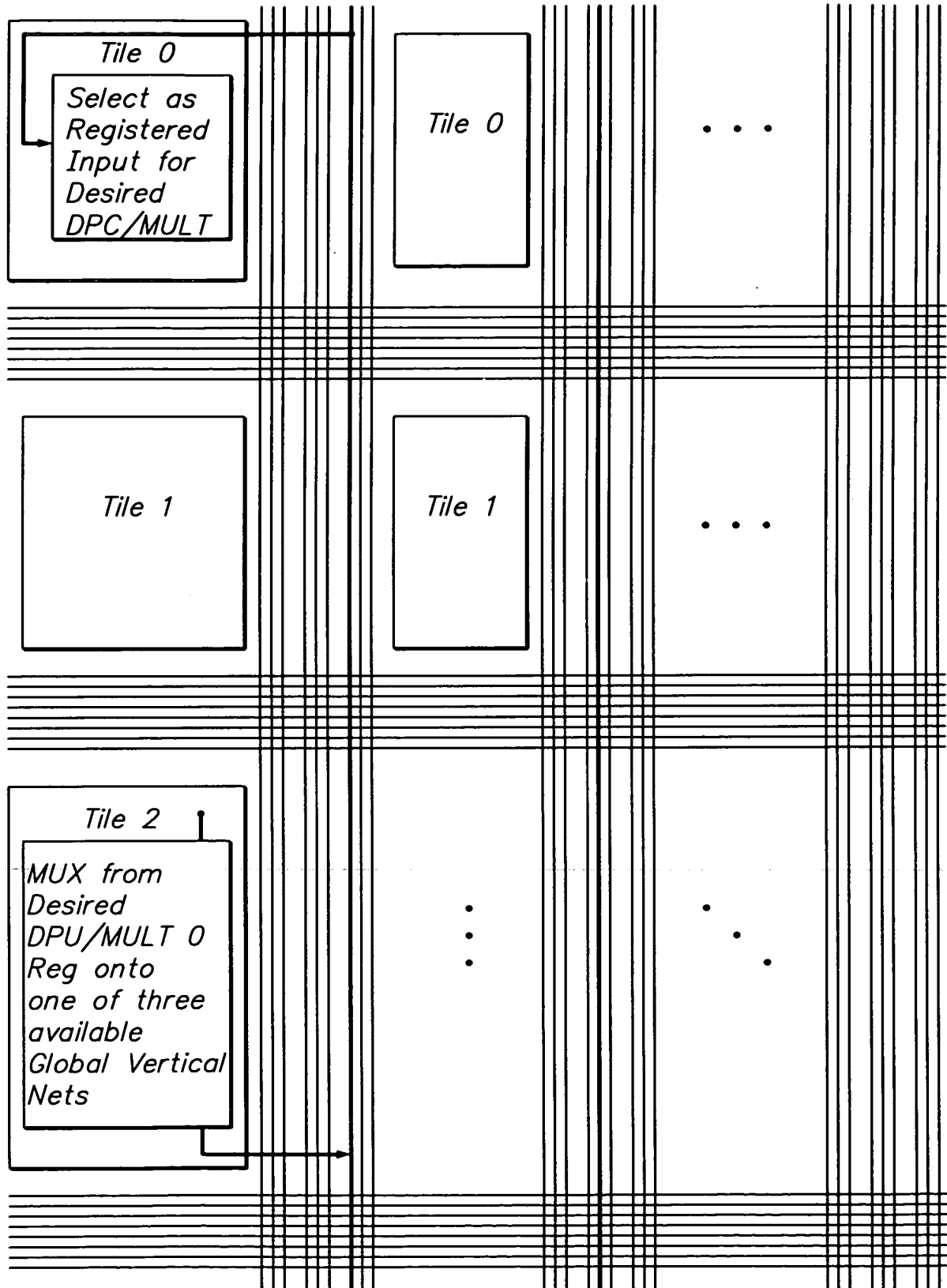


FIG. 9

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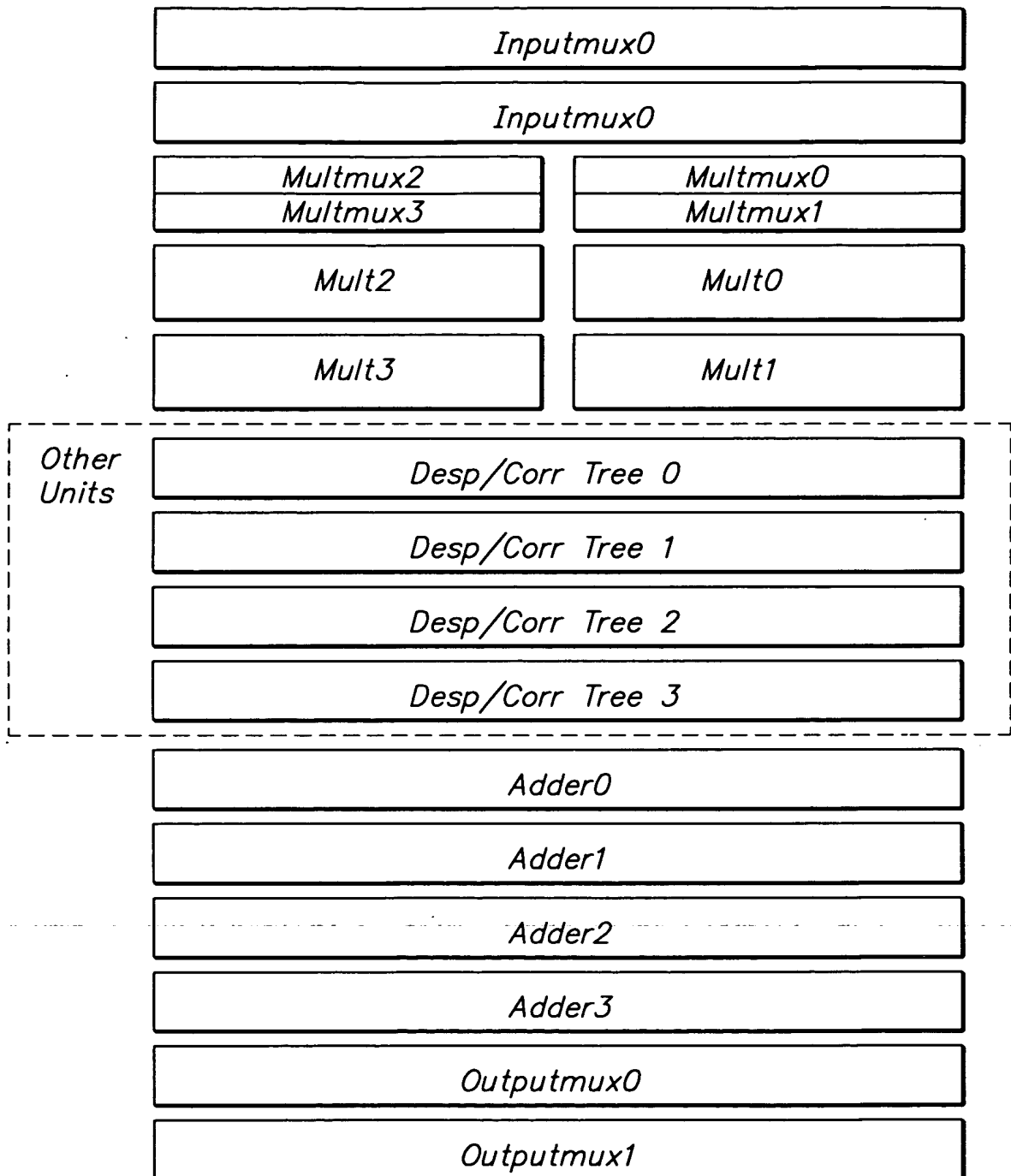


FIG. 10

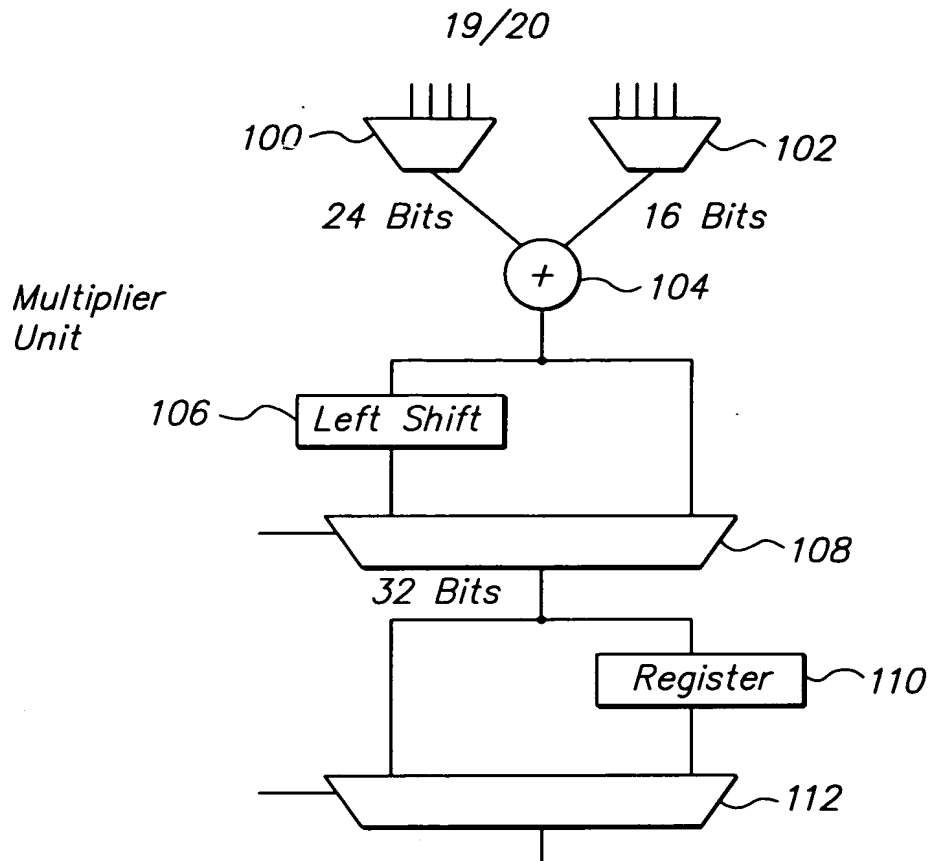


FIG. 11

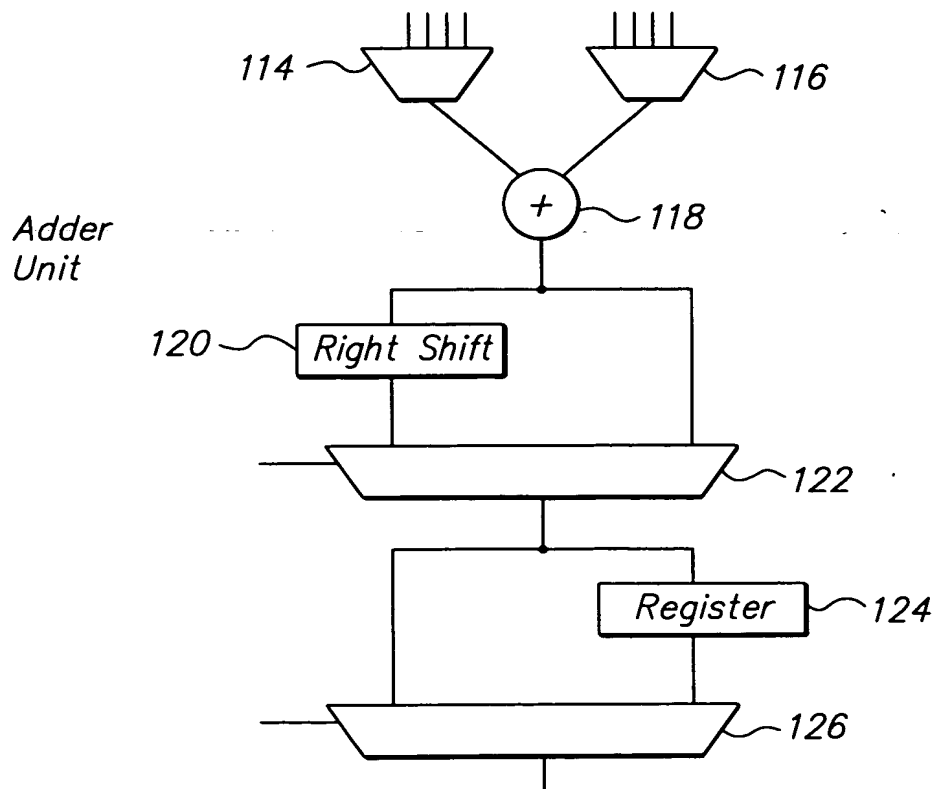


FIG. 12

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The A and B input muxes select from the following sets of 32-bit signals:

16 Local Interconnects (8 previous DPU/MULTs,
 7 next, and DPU Output feedback)

9 Global Vertical nets

3 Reserved

LSM Read Data

LFSR feedback

ALU Output feedback

Logical zero (32'h0)

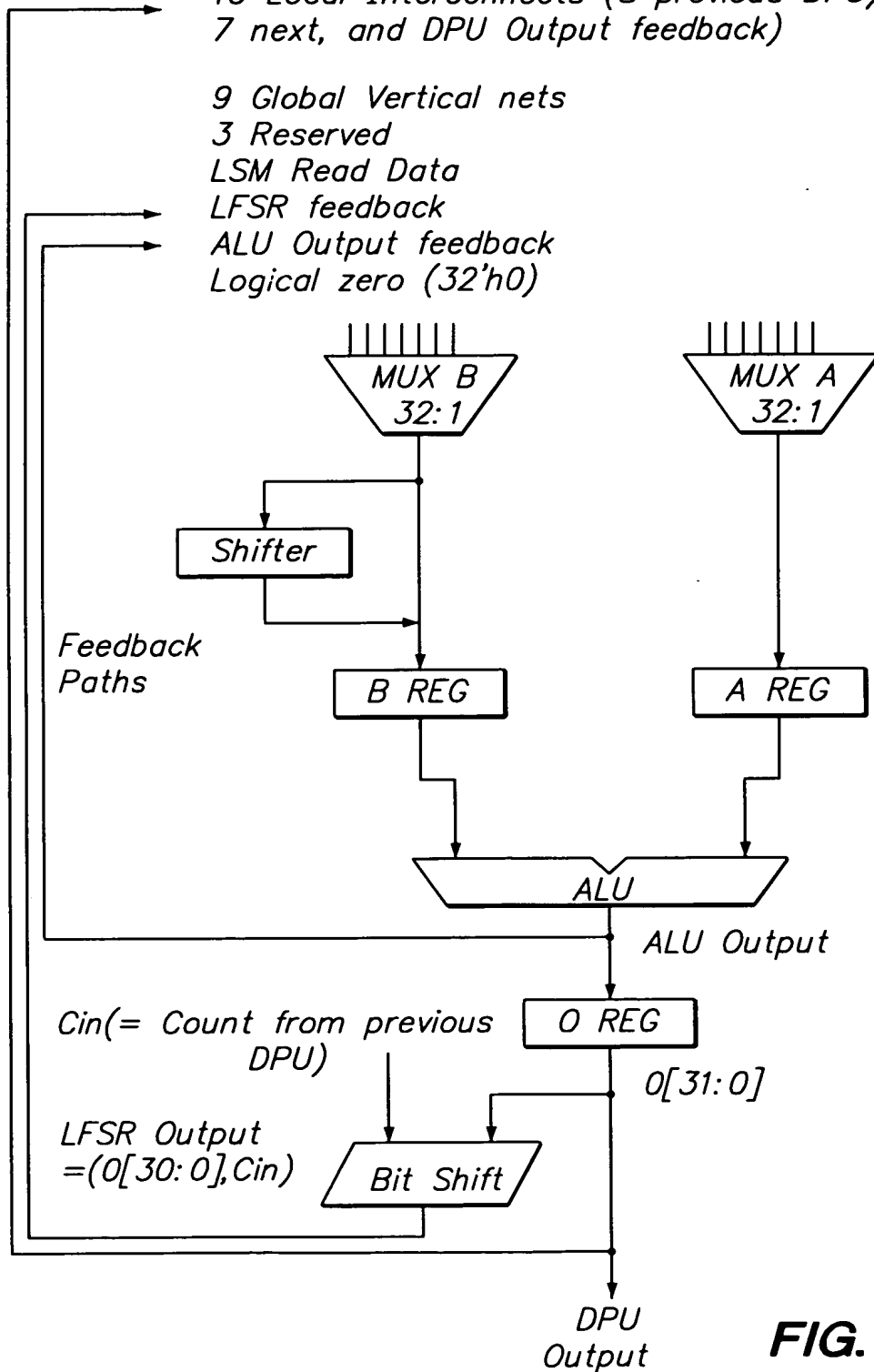


FIG. 13